What is claimed is:

1. A semiconductor device having a lower pattern density in an edge area than in a central area of a wafer, comprising:

a plurality of bar-type patterns allocated at a predetermined distance in the central area of the wafer;

a plurality of dummy patterns formed in the edge area; and

a plurality of a connection pattern adapted to couple at least two of the bar-type patterns to each other and adapted to couple the dummy patterns to each other;

wherein the connection patterns of the plurality of dummy patterns is allocated in a zigzag fashion.

2. The semiconductor device as recited in claim 1, wherein the bar-type pattern is a pattern for a device isolation layer or a landing plug contact.

3. The semiconductor device as recited in claim 2, wherein the dummy pattern includes:

a first bar-type pattern;

a second bar-type pattern allocated at a predetermined distance from the first bar-type pattern; and

the connection pattern adapted to connect the first bar-type pattern to the second bar-type pattern.

4. The semiconductor device as recited in claim 3,

wherein the first and the second bar-type patterns are in a range of about 80% to about 120% of the size of the bar-type pattern.

5. The semiconductor device as recited in claim 1, wherein the dummy pattern includes N number of bar-type patterns allocated at a predetermined distance between two bar-type patterns, where N is a positive integer, and wherein at least two bar-type patterns of the N number of bar-type patterns are connected.

6. The semiconductor device as recited in claim 5, wherein the size of the bar-type patterns is in ranges from about 80% to about 120% of the size of the bar-type pattern.

7. The semiconductor device as recited in claim 1, wherein the central area and the edge area are a cell center area and a cell edge area, respectively.

8. The semiconductor device as recited in claim 1, wherein the central area is a core cell area and the edge area is a peripheral area.